

HDL Simulation using Questa Intel FPGA Edition Installation Instructions



Simulator Options and Licensing

Quartus Prime and Questa Intel FPGA Edition Version Support

Questa Intel FPGA Edition Version	Licensing	Supported Quartus Prime Version	Performance Difference
Questa Intel FPGA Edition version 2023.3	Licenses are required and must be purchased. Each edition supports the same user interface commands, GUI options, and behavior as the Siemens EDA Questa* Core simulator.	Quartus Prime Pro Edition version 23.4 (Windows, Linux)	Reduced speed and instance count ⁽¹⁾ capacity limits in comparison with Siemens EDA Questa* Core.
Questa Intel FPGA Starter Edition 2023.3	Licenses are required but are free. Each edition supports the same user interface commands, GUI options, behavior, and number of module instances as the Siemens EDA Questa* Core simulator.	Quartus Prime Pro Edition version 23.4 (Windows, Linux)	Reduced speed and instance count capacity limits in comparison with Siemens EDA Questa* Core. The Starter Edition has further reduced performance levels.
Questa Intel FPGA Edition version 2023.3	Licenses are required and must be purchased. Each edition supports the same user interface commands, GUI options, and behavior as the Siemens EDA Questa* Core simulator.	Quartus Prime Standard Edition version 23.1 (Windows, Linux)	Reduced speed and instance count capacity limits in comparison with Siemens EDA Questa* Core.
Questa Intel FPGA Starter Edition 2023.3	Licenses are required but are free. Each edition supports the same user interface commands, GUI options, behavior, and number of module instances as the Siemens EDA Questa* Core simulator	Quartus Prime Standard Edition version 23.1 (Windows, Linux)	Reduced speed and instance count capacity limits in comparison with Siemens EDA Questa* Core. The Starter Edition has further reduced performance levels.



Simulator Options and Licensing

Quartus Prime Pro Edition Supported Simulators

Vendor	Simulator	Version	Platform	Supports Siemens EDA Verification IP
Aldec	Active-HDL*	13.0	Windows* 64-bit	No
Aldec	Riviera-PRO*	2023.04	Windows, Linux, 64-bit	No
Cadence	Xcelium* Parallel Simulator	22.09.001	Linux 64-bit	Yes
Siemens EDA	QuestaSim* Simulator ⁽²⁾	2022.4	Windows, Linux, 64-bit	Yes
Synopsys*	VCS*, VCS MX	T-2022.06-SP2-3	Linux 64-bit	Yes



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Select Product & Add Additional Details Add Host & Generate License

Web Description	Maintenance Expiration	License Expiration
<input type="checkbox"/> Intel® Quartus® Prime Software 90-Day Evaluation (Standard and Pro Editions) (License: EVALUATION-LIC)	2024-12-27	2024-12-26
<input type="checkbox"/> Agilix™ 5 E-Series FPGA Software Enablement (License: SW-AGILEX-5E)	2025-09-27	2025-09-27
<input checked="" type="checkbox"/> Questa*-Intel® FPGA Starter Edition (License: SW-QUESTA)	2025-09-27	
<input type="checkbox"/> Nios® V/m Microcontroller Intel® FPGA IP (License: IP-NIOSVM)	2025-09-27	
<input type="checkbox"/> Nios® V/g General Purpose Processor Intel® FPGA IP (License: IP-NIOSVG)	2025-09-27	
<input type="checkbox"/> Nios® V/c Compact Microcontroller Intel® FPGA IP (License: IP-NIOSVC)	2025-09-27	
<input type="checkbox"/> MIPI CSI 2 Intel® FPGA IP (License: IP-MIPI-CSI-2)	2025-09-27	
<input type="checkbox"/> AXI Multichannel DMA for PCI Express (License: IP-PCIEMCDMA-AXI)	2025-09-27	
<input type="checkbox"/> GTS Auto-negotiation/Link Training Feature for Ethernet (License: IP-ETH-ANLT)	2025-09-27	
<input type="checkbox"/> Auto-Negotiation/Link Training Feature F-Tile Hard IP for Ethernet (License: IP-ETH-F-ANLT)	2025-09-27	
<input type="checkbox"/> F-Tile Hard IP for Ethernet, supporting from 10G to 400G Ethernet with optional 1588 PTP feature (License: IP-ETH-FTILEHIP)	2025-09-27	
<input type="checkbox"/> KR/CR (AN/LT) for H-tile Ethernet HIP (100GE) (License: IP-ETH-HTILEKRCR)	2025-09-27	
<input type="checkbox"/> H-tile Ethernet Hard-IP (100GE) (License: IP-ETH-HTILEHIP)	2025-09-27	
<input type="checkbox"/> E-tile Ethernet Hard-IP (10GE/25GE/100GE) (License: IP-ETH-ETILEHIP)	2025-09-27	
<input type="checkbox"/> Discontinued - Nios® II/f Processor Intel® FPGA IP (License: IP-NIOS)	2024-12-27	
<input type="checkbox"/> Discontinued - MAX+PLUS® II Software License for Student and University Members (License: PLS-WEB)	2025-09-27	
<input type="checkbox"/> Discontinued - Intel® Quartus® II Software (License: SW-QUARTUS-WE-FIX)	2025-09-27	
<input type="checkbox"/> Discontinued - MAX+PLUS® II Software (License: MAXPLUS2WEB)	2025-09-27	

* # of Seats

Next License Assistant



Obtaining Questa Intel License

The screenshot shows the Intel FPGA Self-Service Licensing Center interface. At the top, there is a navigation bar with the Intel logo and links for PRODUCTS, SUPPORT, SOLUTIONS, DEVELOPERS, PARTNERS, and FOUNDRY. Below this is a sub-header for 'Intel® FPGA Self-Service Licensing Center' with a secondary navigation bar containing Home, Licenses, Computers and License Files, Admins, Sign up for Evaluation or No-Cost Licenses, Reports, and Help. A progress bar indicates the current step is 'Add Host & Generate License'. The main heading is '* Generate License (Create a New Computer Or Choose an Existing Computer)'. Underneath, there is a section for 'Choose an Existing Computer' with a search box containing 'EC6307D2DDAE' and a 'View All Computers' link. A modal window titled 'Create Computer' is open, containing the following fields: '* Computer Name' (text input with 'Student'), '* License Type' (dropdown menu with 'FIXED'), 'Companion Computer ID 1' (text input), '* Primary Admin' (text input with 'Dina Eldamak'), '* Computer Type' (dropdown menu with 'NIC ID'), and '* Primary Computer ID' (text input, highlighted with a red box). A tooltip for the Primary Computer ID field reads 'How to find your hardware information (NIC/Host/Guard ID)?'. Other fields include 'Companion Computer ID 2' (text input). At the bottom of the modal are 'Cancel' and 'Save' buttons. The footer of the page includes 'Company Overview', 'Contact Intel', 'Newsroom', 'Investors', 'Careers', 'Corporate Responsibility', 'Diversity & Inclusion', and 'Public Policy', along with social media icons and legal disclaimers.



Finding Computer ID

```
Command Prompt
Microsoft Windows [Version 10.0.22631.41]
(c) Microsoft Corporation. All rights reserved.

C:\Users\dina>ipconfig/all

Windows IP Configuration

Host Name . . . . . : Dina-PC
Primary Dns Suffix . . . . . :
Node Type . . . . . : Hybrid
IP Routing Enabled. . . . . : No
WINS Proxy Enabled. . . . . : No

Ethernet adapter Ethernet:

Media State . . . . . : Media disconnected
Connection-specific DNS Suffix . . . . . :
Description . . . . . : Realtek PCIe GbE Family Controller
Physical Address. . . . . : 68-8E-8E-8E-8E-8E
DHCP Enabled. . . . . : Yes
Autoconfiguration Enabled . . . . . : Yes

Wireless LAN adapter Local Area Connection 2:

Media State . . . . . : Media disconnected
Connection-specific DNS Suffix . . . . . :
Description . . . . . : Realtek PCIe GbE Family Controller
```

The 'Create Computer' dialog box shows the following fields:

- Computer Name: Student
- License Type: FIXED
- Computer Type: NIC ID
- Primary Admin: Dina Eldamak
- Physical Address: (empty)

```
Wireless LAN adapter Wi-Fi:

Connection-specific DNS Suffix . . . . . :
Description . . . . . : Realtek PCIe GbE Family Controller
Physical Address. . . . . : XX-XX-XX-XX-XX-XX
DHCP Enabled. . . . . : Yes
Autoconfiguration Enabled . . . . . : Yes
```

Remove the dashes before you enter the physical address in create computer

Generate License and obtain it by email



Download Intel Questa Software

Downloads

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Intel® Quartus® Software

Quartus® Prime (includes Nios II EDS)

Download
QuartusLiteSetup-23.1std.1.993-windows.exe

Size: 1.6 GB

SHA1:

ad8fb45076b42f332f46264ccaeb3af8e34
829de

** Installation size: 8.55 GB

Questa*-Intel® FPGA and Starter Editions

Download
QuestaSetup-23.1std.1.993-windows.exe

Size: 802.4 MB

SHA1:

ba612aec6a697ec0b3643e8c61e084346
06093e

** Installation size: 3.31 GB

<https://www.intel.com/content/www/us/en/software-kit/825278/intel-quartus-prime-lite-edition-design-software-version-23-1-1-for-windows.html>



Check your C: Folder

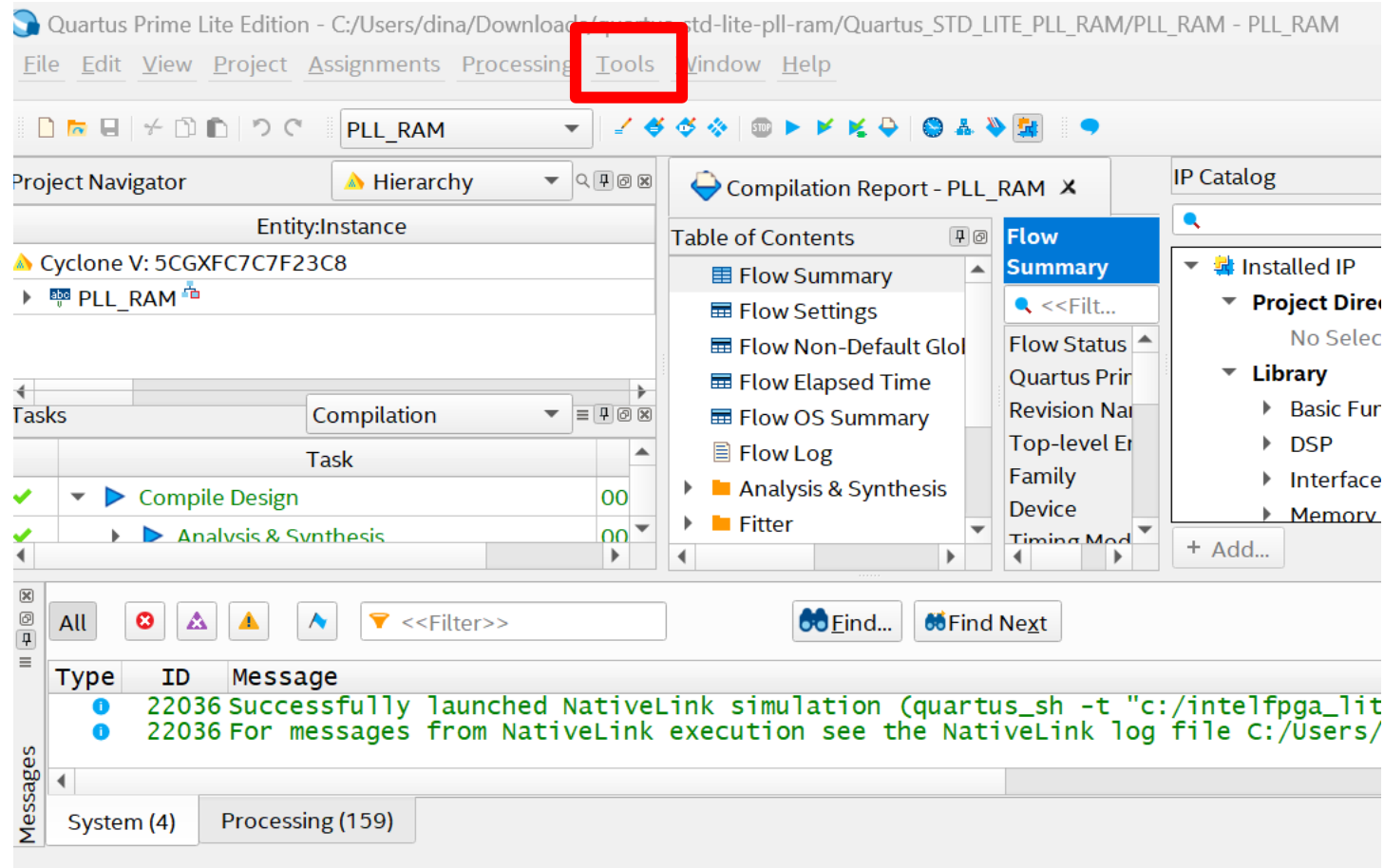
This screenshot shows the Windows File Explorer interface for the Local Disk (C:). The address bar indicates the path: This PC > Local Disk (C:) >. The main area displays a list of folders with columns for Name, Date modified, Type, and Size. The folders 'intelFPGA' and 'intelFPGA_lite' are highlighted with a red rectangular box. Blue arrows point from these folders to descriptive text labels.

Name	Date modified	Type	Size
flexlm	9/20/2024 9:48 AM	File folder	
Intel	9/27/2024 11:09 AM	File folder	
intelFPGA	9/27/2024 11:02 AM	File folder	
intelFPGA_lite	9/27/2024 11:02 AM	File folder	
PerfLogs	5/7/2022 7:24 AM	File folder	
Program Files	9/20/2024 10:27 AM	File folder	
Program Files (x86)	7/20/2024 3:17 PM	File folder	
Users	12/25/2022 11:59 PM	File folder	
Windows	9/20/2024 10:20 AM	File folder	



Setup Intel Questa

Open Intel Quartus



Setup Intel Questa

Quartus Prime Lite Edition - C:/Users/dina/Download

File Edit View Project Assignments Processing

PLL_RAM

Project Navigator Hierarchy

Entity: Instance

Cyclone V: 5CGXFC7C7F23C8

PLL_RAM

Tasks Compilation

Task

Compile Design

Analysis & Synthesis

Messages

Type	ID	Message
Info	22036	Successfully launched Native
Info	22036	For messages from Native

System (4) Processing (159)

Options...

Options

Category: General

EDA Tool Options

Specify the directory that contains the tool executable for each third-party EDA tool:

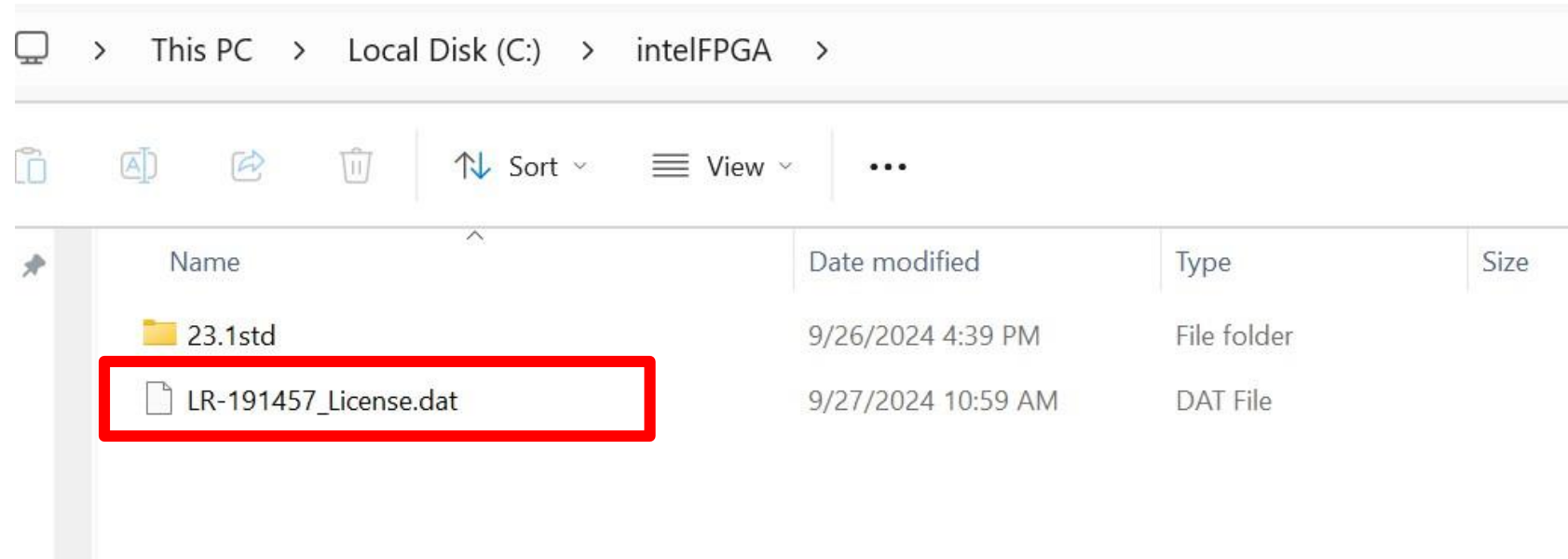
EDA Tool	Directory Containing Tool Executable
Precision Synth...	...
Synplify	...
Synplify Pro	...
Active-HDL	...
Riviera-PRO	...
ModelSim	...
Questa Intel FP...	C:/intelFPGA/23.1std/questa_fse/win64

OK Cancel Help

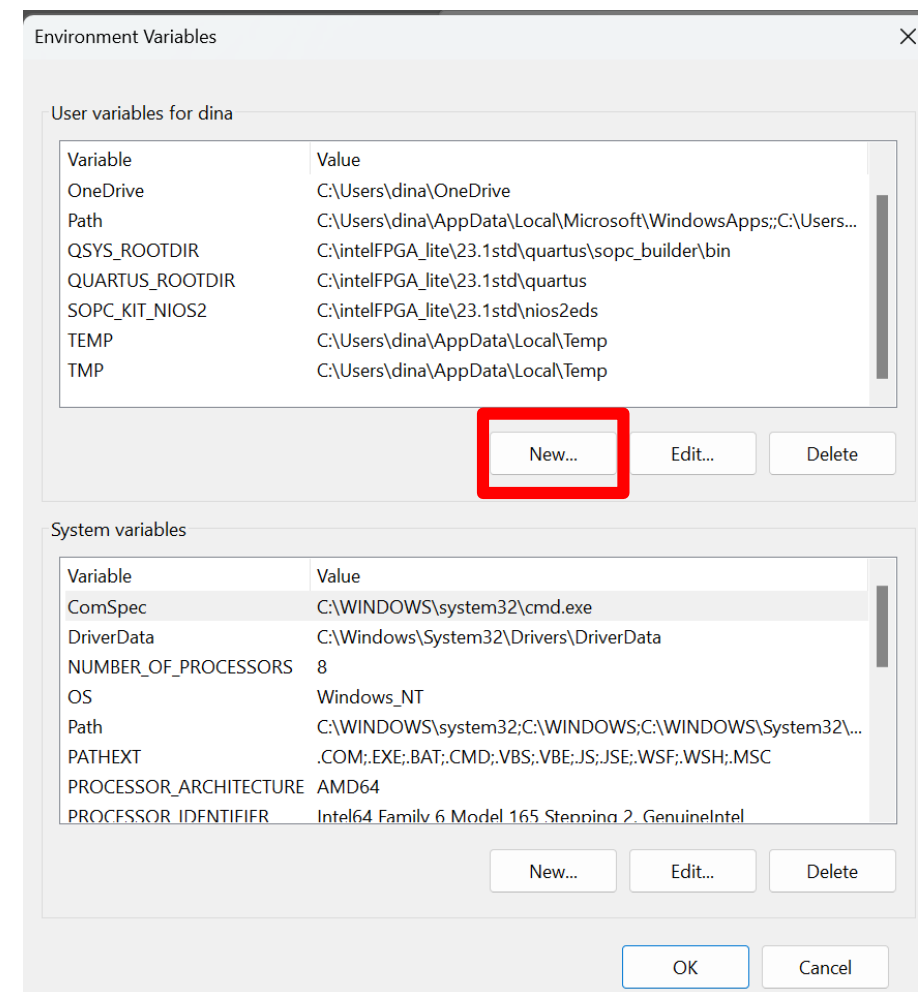
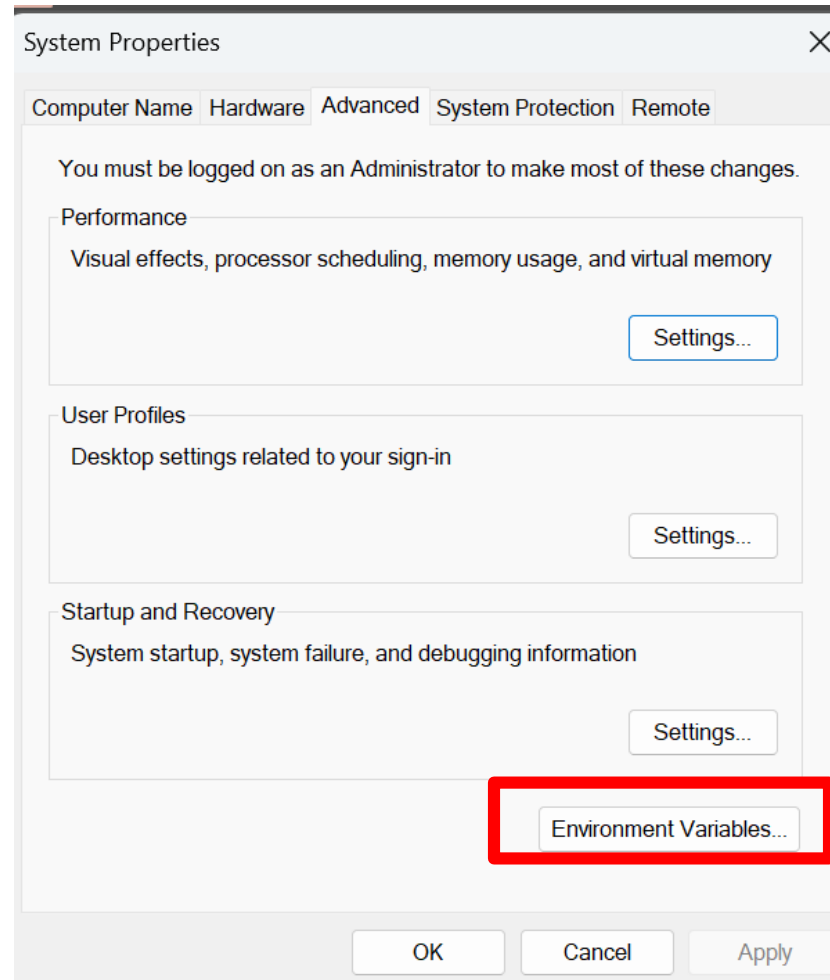
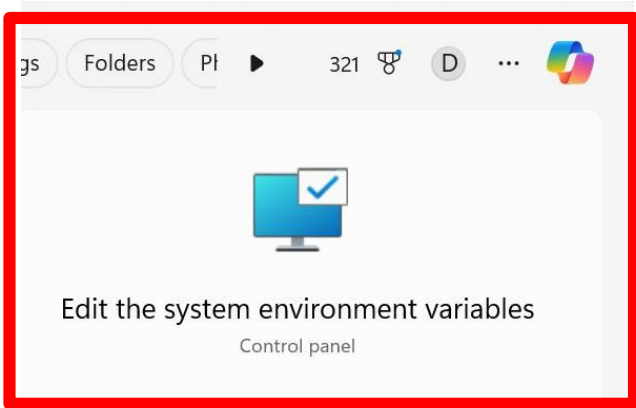


Adding License File

Copy license file to intelFPGA folder



Adding License File



Adding License File

New User Variable

Variable name: LM_LICENSE_FILE

Variable value: C:\intelFPGA\LR-191457_License.dat

Browse Directory... Browse File... **OK** Cancel

Environment Variables

User variables for dina

Variable	Value
LM_LICENSE_FILE	C:\intelFPGA\LR-191457_License.dat
Path	C:\Users\dina\AppData\Local\Microsoft\WindowsApps;;C:\Users...
QSYS_ROOTDIR	C:\intelFPGA_lite\23.1std\quartus\sopc_builder\bin
QUARTUS_ROOTDIR	C:\intelFPGA_lite\23.1std\quartus
SOPC_KIT_NIOS2	C:\intelFPGA_lite\23.1std\nios2eds
TEMP	C:\Users\dina\AppData\Local\Temp
TMP	C:\Users\dina\AppData\Local\Temp

New... Edit... Delete

System variables

Variable	Value
ComSpec	C:\WINDOWS\system32\cmd.exe
DriverData	C:\Windows\System32\Drivers\DriverData
NUMBER_OF_PROCESSORS	8
OS	Windows_NT
Path	C:\WINDOWS\system32;C:\WINDOWS;C:\WINDOWS\System32\...
PATHEXT	.COM;.EXE;.BAT;.CMD;.VBS;.VBE;.JS;.JSE;.WSF;.WSH;.MSC
PROCESSOR_ARCHITECTURE	AMD64
PROCESSOR_IDENTIFIER	Intel64 Family 6 Model 165 Stepping 2, GenuineIntel

New... Edit... Delete

OK Cancel



Launch Intel Questa

Restart windows then launch Intel Quartus

Quartus Prime Lite Edition - C:/Users/dina/Downloads/quartus-std-lite-pll-ram/Quartus_STD_LITE_PLL_RAM/PLL_RAM - PLL_RAM

File Edit View Project Assignments Processing Tools Window Help

Run Simulation Tool
Launch Simulation Library Compiler
Launch Design Space Explorer II
Timing Analyzer
Advisors
Chip Planner
Design Partition Planner
Netlist Viewers
Signal Tap Logic Analyzer
In-System Memory Content Editor
Logic Analyzer Interface Editor
In-System Sources and Probes Editor
Signal Probe Pins...
Programmer
JTAG Chain Debugger
Fault Injection Debugger
System Debugging Tools
IP Catalog
Nios II Software Build Tools for Eclipse
Platform Designer
Tcl Scripts...
Customize...
Options...
License Setup...
Install Devices...

RTL Simulation
Gate Level Simulation...

Project Navigator: Hierarchy
Entity: Instance
Cyclone V: 5CGXFC7C7F23C8
PLL_RAM

Tasks: Compilation
Task: Compile Design
Analysis & Synthesis

Messages: System Processing
Runs the specified RTL simulation tool
steps:
5. View Signal Waveform
Follow these steps
6. Add Signals to the Waveform
The CLOCK, WE, OFF...
addition, you can o...
7. Rerun Simulation

You must rerun the simulation if you make changes to the simulation setup, such as adding signals to the Wave window, testbench.tcl file. Follow these steps to rerun simulation:



Launch Intel Questa

The screenshot displays the Intel Questa Starter FPGA Edition-64 2023.3 software interface. The main window is titled "sim - Default" and shows a simulation in progress. The "Wave - Default" window displays a timing diagram with a cursor at 4030 ns. The "Objects" window shows a list of design units and their types. The "Processes (Active)" window shows the active processes during the simulation. The "Transcript" window shows the simulation log, including a note about the simulation time and a break in the module.

QuestaIntel Starter FPGA Edition-64 2023.3

File Edit View Compile Simulate Add Wave Tools Layout Bookmarks Window Help

Layout Simulate ColumnLayout AllColumns

sim - Default

Instance Design unit Design

Instance	Design unit	Design
tb	tb(fast)	Modu
Test1	PLL_RAM(f...	Modu
dock_modu...	ClockPLL(fa...	Modu
UP_module	UP_COUNT...	Modu
DOWN_mo...	DOWN_CO...	Modu
RAM_modul...	RAMhub(fast)	Modu
#ASSIGN#...	PLL_RAM(f...	Proce
#ALWAYS#23	tb(fast)	Proce
#INITIAL#27	tb(fast)	Proce
std	std	VIPad
altera_insi...	altera_insi...	VIPad
altera_generi...	altera_gen...	VIPad
#vsim_capacity#		Capa

Objects

Name	Type
locked	1'h1 Net
outdk_0	1'h0 Net
outdk_1	1'h0 Net
refck	1'h0 Net
rst	1'h0 Net
wire_dockpll_altera...	1'h1 Net
wire_dockpll_altera...	2'h0 Net

Processes (Active)

Name	Type (filtered)
#INITIAL#27	Initial
#ALWAYS#23	Always
#ALWAYS#1968	Always

Wave - Default

Msgs	Value
/tb/CLOCK	1'h0
/tb/WE	1'h1
/tb/OFFSET	8'h1c
/tb/RESET_N	1'h0
/tb/RD_DATA	9'h0ba
/tb/Test1/RAM_mo...	8'h9c
/tb/Test1/RAM_mo...	8'h2c

Transcript

```
# ** Note: $stop : C:/Users/dina/Downloads/quartus-std-lite-pll-ram/Quartus_STD_LITE_PLL_RAM/testbench_1.v(46)
# Time: 4030 ns Iteration: 0 Instance: /tb
# Break in Module tb at C:/Users/dina/Downloads/quartus-std-lite-pll-ram/Quartus_STD_LITE_PLL_RAM/testbench_1.v line 46
VSIM 7>
```

Now: 4,030 ns Delta: 0

tb

4028508 ps to 4030079 ps

VHDL Simulation using Questa Intel FPGA Edition Tutorial



Create New Project

The screenshot shows the Quartus Prime Lite Edition software interface. The 'File' menu is open, and 'New Project Wizard...' is selected. The main workspace displays a 'Recent Projects' section with two entries: 'PLL_RAM.qpf' and 'lane.qpf'. Below this, there are buttons for 'New Project Wizard' and 'Open Project'. At the bottom of the workspace, there are links for 'Tutorial Video: 28G Transceivers', 'Tutorial Video: Hyperflex Architecture', and 'Tutorial Video: PCIeGen2 DMA to DDR4'. The right sidebar shows the 'IP Catalog' for 'Cyclone V (E/GX/GT/SX/SE/ST)' with a tree view of installed IP components.

Quartus Prime Lite Edition

File Edit View Project Assignments Processing Tools Window Help

New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Save Project
Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4

Home x

Recent Projects

- PLL_RAM.qpf (C:/Users/dina/Downloads/quartus-st...e-pll-ram/Quartus_STD_LITE_PLL_RAM/PLL_RAM.qpf)
- lane.qpf (C:/Users/dina/Documents/Intelfpga/lane_detection/lane.qpf)

New Project Wizard Open Project

Compare Editions Buy Software Documentation Training Support What's New

Tutorial Video: [28G Transceivers](#)
Tutorial Video: [Hyperflex Architecture](#)
Tutorial Video: [PCIeGen2 DMA to DDR4](#)

Close page after project load
 Don't show this screen again

intel

IP Catalog
Device Family Cyclone V (E/GX/GT/SX/SE/ST)

Installed IP

- Project Directory
No Selection Available
- Library
 - Basic Functions
 - DSP
 - Interface Protocols
 - Memory Interfaces and Controllers
 - Processors and Peripherals
 - University Program
- Search for Partner IP

+ Add...



Create New Project

Directory, Name, Top-Level Entity

What is the working directory for this project?

C:/Users/dina/Documents/Intelfpga/full_adder ...

What is the name of this project?

full_adder ...

What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.

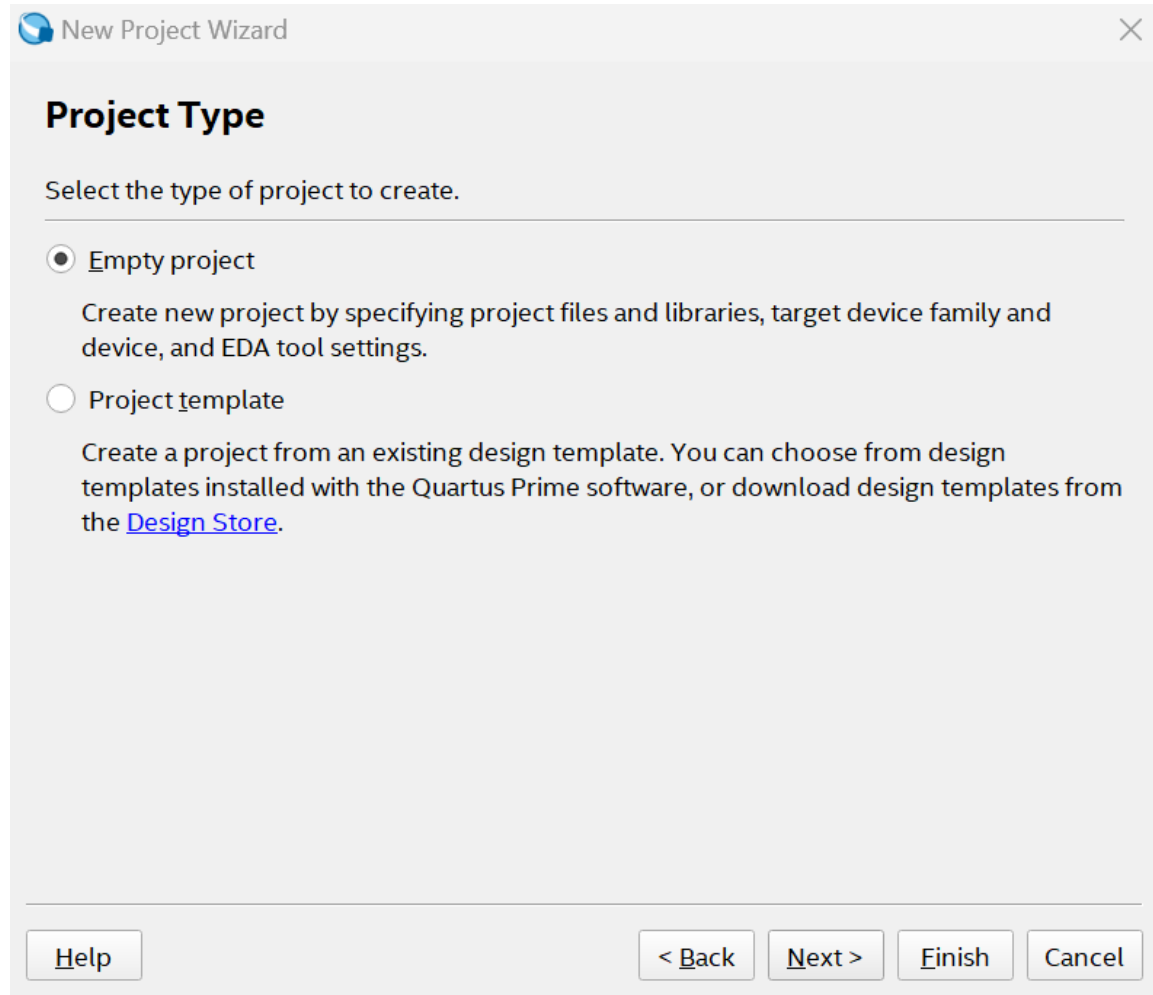
full_adder ...

Use Existing Project Settings...

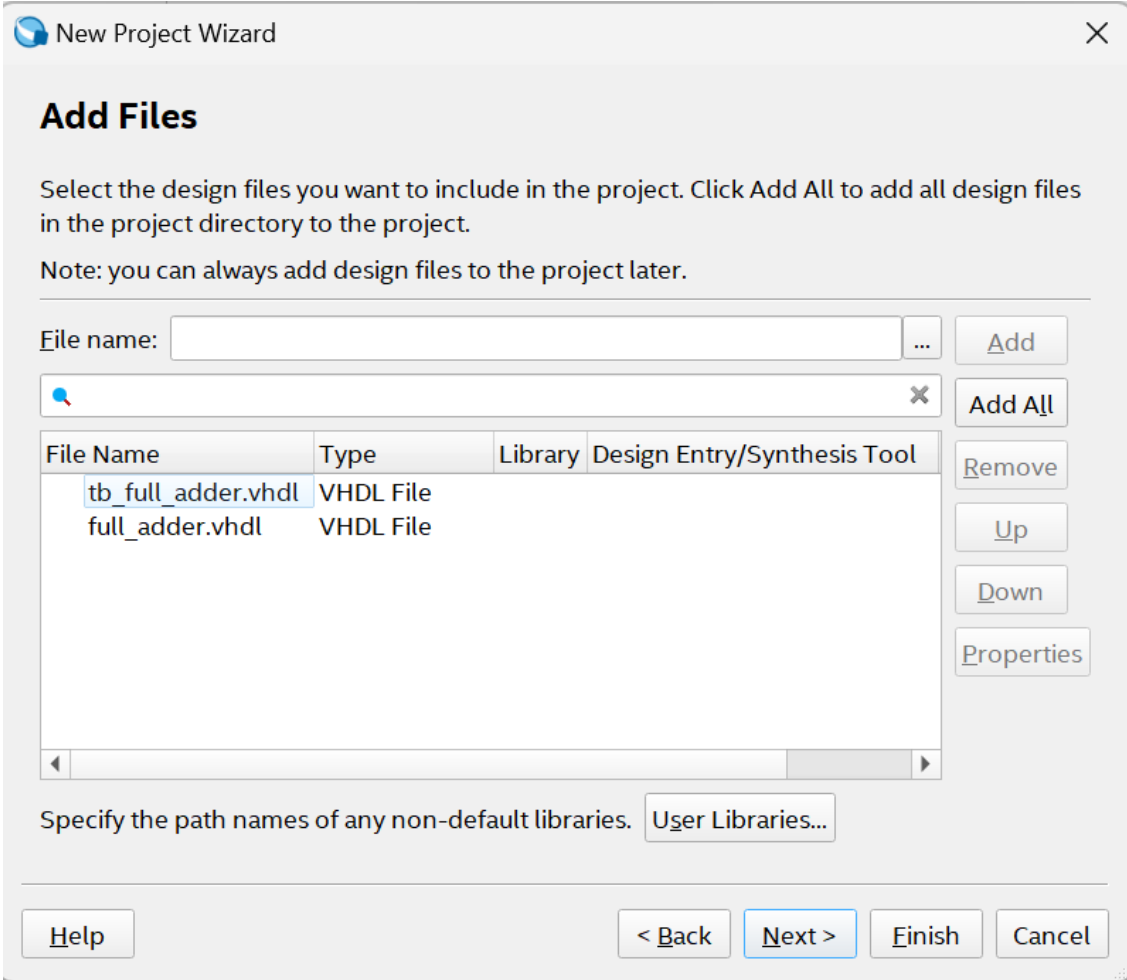
Help < Back Next > Finish Cancel



Create New Project



Add VHDL Files



Select FPGA

New Project Wizard

Family, Device & Board Settings

Device Board

Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.

To determine the version of the Quartus Prime software in which your target device is supported, refer to the [Device Support List](#) webpage.

Device family

Family: Cyclone V (E/GX/GT/SX/SE/ST)
Device: All

Target device

Auto device selected by the Fitter
 Specific device selected in 'Available devices' list
 Other: n/a

Show in 'Available devices' list

Package: Any
Pin count: Any
Core speed grade: Any

Name filter: 5CEBA2F17C6
 Show advanced devices

Available devices:

Name	Core Voltage	ALMs	Total I/Os	GPIOs	GXB Channel PMA	GXB Channel PCS	PCIe Hard I
5CEBA2F17C6	1.1V	9430	128	128	0	0	0

Help < Back Next > Finish Cancel



EDA Tools Settings

New Project Wizard

EDA Tool Settings

Specify the other EDA tools used with the Quartus Prime software to develop your project.

EDA tools:

Tool Type	Tool Name	Format(s)	Run Tool Automatically
Design Entry/Synt...	<None>	<None>	<input type="checkbox"/> Run this tool automatically to synthesize the current design
Simulation	Questa Intel FPGA	VHDL	<input type="checkbox"/> Run gate-level simulation automatically after compilation
Board-Level	Timing	<None>	
	Symbol	<None>	
	Signal Integrity	<None>	
	Boundary Scan	<None>	

Help < Back Next > Finish Cancel



View the VHDL Code and start compilation

The screenshot displays the Quartus Prime Lite Edition interface. The main window shows the VHDL code for a full adder entity. The code is as follows:

```
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3
4 entity full_adder is
5   Port ( A : in STD_LOGIC;
6         B : in STD_LOGIC;
7         Cin : in STD_LOGIC;
8         S : out STD_LOGIC;
9         Cout : out STD_LOGIC);
10 end full_adder;
11
12 architecture gate_level of full_adder is
13
14 begin
15
16   S <= A XOR B XOR Cin ;
17   Cout <= (A AND B) OR (Cin AND A) OR (Cin AND B) ;
18
19 end gate_level;
```

The toolbar at the top contains several icons, with the 'Run' icon (a play button) highlighted by a red box. The Project Navigator on the left shows the project hierarchy for 'Cyclone V: 5CEBA2F17C6', with 'full_adder' selected. The Tasks window at the bottom left shows the 'Compilation' task list, which includes 'Compile Design', 'Analysis & Synthesis', 'Fitter (Place & Route)', 'Assembler (Generate programming files)', 'Timing Analysis', and 'EDA Notlist Writer'. The IP Catalog on the right shows the installed IP libraries, including 'Project Directory', 'Library', and 'Search for Partner IP'.



Setup the testbench

The screenshot displays the Quartus Prime Lite Edition interface. The main window shows the 'Flow Summary' for a successful compilation on Friday, September 27, 2024, at 14:40:22. The summary includes details such as the Quartus Prime Version (23.1std.1), Revision Name (full_adder), Top-level Entity Name (full_adder), Family (Cyclone V), and Device (5CEBA2F17C6). Resource utilization statistics are provided, including logic utilization (2 / 9,430 ALMs, < 1%), total registers (0), total pins (5 / 128, 4%), and total virtual pins (0). Block memory usage is 0 / 1,802,240 bits (0%), and DSP blocks are 0 / 25 (0%). HSSI RX PCSs, HSSI PMA RX Deserializers, HSSI TX PCSs, HSSI PMA TX Serializers, PLLs, and DLLs are all reported as 0 / 4 (0%).

The 'Assignments' menu is open, showing options like 'Settings...', 'Assignment Editor', 'Pin Planner', and 'Logic Lock Regions Window'. The 'Tasks' window shows the compilation process completed successfully, with sub-tasks like 'Compile Design', 'Analysis & Synthesis', 'Fitter (Place & Route)', 'Assembler (Generate programming files)', 'Timing Analysis', and 'EDA Netlist Writer' all marked with green checkmarks.

The 'IP Catalog' window is visible on the right, showing the 'Installed IP' section with a 'Project Directory' and a 'Library' containing various components like 'Basic Functions', 'DSP', 'Interface Protocols', 'Memory Interfaces and Controllers', 'Processors and Peripherals', and 'University Program'. A 'Search for Partner IP' button is also present.



Settings - full_adder

Category: Device/Board...

- General
- Files
- Libraries
- IP Settings
 - IP Catalog Search Locat
- Design Templates
- Operating Settings and Cor
 - Voltage
 - Temperature
- Compilation Process Settin
 - Incremental Compilatio
- EDA Tool Settings
 - Design Entry/Synthesis
 - Simulation
 - Board-Level
- Compiler Settings
 - VHDL Input
 - Verilog HDL Input
 - Default Parameters
- Timing Analyzer
- Assembler
- Design Assistant
- Signal Tap Logic Analyzer
- Logic Analyzer Interface
- Power Analyzer Settings
- SSN Analyzer

Simulation

Specify options for generating output files for use with other EDA tools.

Tool name: Questa Intel FPGA

Run gate-level simulation automatically after compilation

EDA Netlist Writer settings

Format for output netlist: VHDL Time scale: 100 us

Output directory: simulation/questa

Map illegal HDL characters Enable glitch filtering

Options for Power Estimation

Generate Value Change Dump (VCD) file script Script Settings...

Design instance name:

More EDA Netlist Writer Settings...

NativeLink settings

None

Compile test bench: Testbench_full_adder Test Benches...

Use script to set up simulation:

Script to compile test bench:

More NativeLink Settings... Reset

Buy Software OK Cancel Apply Help

Test Benches

Specify settings for each test bench.

Existing test bench settings: New...

Name	Top Level Module	Design Instance	Run For	Edit...
Testbench_full...	Testbench_full...	NA	170 ns	Delete

OK Cancel Help



Setup the testbench

New Test Bench Settings

Create new test bench settings.

Test bench name: Testbench_full_adder

Top level module in test bench: Testbench_full_adder

Use test bench to perform VHDL timing simulation

Design instance name in test bench: NA

Simulation period

Run simulation until all vector stimuli are used

End simulation at: 170 ns

Test bench and simulation files

File name: tb_full_adder.vhdl ... Add

File Name	Library	HDL Version
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Remove
Up
Down
Properties...

OK Cancel Help



Setup the testbench

The screenshot shows the 'Settings - full_adder' dialog box with the 'Simulation' category selected. The 'Simulation' section is active, showing options for tool name, simulation options, and EDA Netlist Writer settings. A 'New Test Bench Settings' dialog is overlaid on top, with the following fields and options:

- Test bench name: Testbench_full_adder
- Top level module in test bench: Testbench_full_adder
- Use test bench to perform VHDL timing simulation
- Design instance name in test bench: NA
- Simulation period:
 - Run simulation until all vector stimuli are used
 - End simulation at: 170 ns
- Test bench and simulation files:
 - File name: [empty]
 - Table with columns: File Name, Library, HDL Version
 - Table content: tb_full_adder.v..., [empty], Default
 - Buttons: Add, Remove, Up, Down, Properties...
- Buttons: OK (highlighted in red), Cancel, Help



View the outputs using Questa

The screenshot displays the Questa tool interface for a simulation. The main window shows a timing diagram for a full adder circuit. The signals being monitored are A, B, Cin, S, and Cout. The timing diagram shows the signals changing over time, with a cursor positioned at 110.662 ns. The transcript window at the bottom shows the simulation progress and a message indicating that the causality operation was skipped due to the absence of a debug database file.

Signal	Value
/testbench_full_adder/A	0
/testbench_full_adder/B	1
/testbench_full_adder/Cin	0
/testbench_full_adder/S	1
/testbench_full_adder/Cout	0

Transcript:

```
# .main_pane.objects.interior.cs.body.tree  
# run 170 ns  
# Causality operation skipped due to absence of debug database file  
VSIM 2>
```

Now: 170 ns Delta: 1 sim:/testbench_full_adder 119657 ps to 120590 ps



Thank you

